IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): D.B. Kramer et al.
Case: 7-20
Serial No.: 10/085,219
Filing Date: February 28, 2002
Group: 2616
Examiner: Rhonda L. Murphy

Title: Processor With Dynamic Table-Based Scheduling Using Linked Transmission Elements For Handling Transmission Request Collision

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter "Appellants") hereby appeal the final rejection dated December 29, 2006 of claims 1-15 and 18-22 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned of record to Agere Systems Inc. On April 2, 2007, the assignee Agere Systems Inc. completed a merger with LSI Logic Corporation, with the resulting entity being named LSI Corporation. LSI Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on February 28, 2002 with claims 1-22. Claims 1-22 remain pending. Claims 1, 16, 17, 21 and 22 are the independent claims. Claims 16 and 17 are allowed.

Each of claims 1-15 and 18-22 stands rejected under 35 U.S.C. §103(a). Claims 1-15 and 18-22 are appealed.

STATUS OF AMENDMENTS

In a previous response dated March 29, 2007, Appellants proposed an amendment to claim 22 solely to comply with a requirement of form expressly set forth in the present final Office Action dated December 29, 2006, thereby presenting claim 22 in better form for consideration on appeal, in compliance with 37 C.F.R. §§1.116(b)(1) and (b)(2). Specifically, in the final Office Action dated December 29, 2006, the Examiner objected to the recitation of a "machine-readable medium" as an informality and suggested that it be changed to "computer-readable medium."

Appellants submit that the recited article of manufacture comprising a machine-readable storage medium for use in conjunction with a processor, the medium storing one or more software programs that, when executed, perform one or more steps producing a concrete, useful, and tangible result, constitutes a proper claim of statutory subject matter. See, e.g., In re Beauregard, 53 F.3d 1583, 35 USPQ2d 1383 (Fed. Cir. 1995); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Notwithstanding the traversal, Appellants agreed to amend independent claim 22 without prejudice, solely in order to expedite prosecution of the application, so as to recite a computer-readable storage medium, rather than a machine-readable storage medium.

In an Advisory Action dated April 19, 2007, the Examiner indicated that the proposed amendment would not be entered without indicating any reasons for non-entry, in contravention of MPEP § 714.13: "The refusal to enter the proposed amendment should not be arbitrary. The proposed amendment should be given sufficient consideration . . . . The reasons for nonentry should be concisely expressed."

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a processor that comprises scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements and traffic shaping circuitry coupled to the scheduling circuitry and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements. The scheduling circuitry is configured for utilization of at least one time slot table comprising a plurality of locations, each corresponding to a transmission time slot and being configured to store at least one entry. The scheduling circuitry is operative in conjunction with the time slot table to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by the traffic shaping circuitry in the presence of collisions between requests from the transmission elements for each of one or more of the time slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

In an illustrative embodiment, shown in FIG. 3 of the drawings and described in the specification at, for example, page 6, line 1, to page 8, line 22, and page 16, lines 13-22, processor 102 comprises scheduler 306 for scheduling data blocks for transmission from a plurality of transmission elements (e.g., those associated with transmit queue 302) and traffic shaping engine 304 coupled to scheduler 306 and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements. Scheduler 306 is configured for utilization of at least one time slot table 308 comprising a plurality of locations, each corresponding to a transmission time slot and being configured to store at least one entry. As discussed in the specification, with reference to FIG. 7 of the drawings, at, for example, page 14, line 9 to page 16, line 12, scheduler 306 is operative in conjunction with time slot table 308 to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by traffic shaping engine 304 in the presence of collisions between requests from the transmission elements for each of one or more of the time slots, through the use of a linking of colliding transmission elements and by moving

at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

Independent claim 21 is a directed to a method for use in a processor for scheduling data blocks for transmission from a plurality of transmission elements. The method comprises a step of establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements. The method further comprises a step of scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more transmission time slots. This step utilizes at least one time slot table comprising a plurality of locations, each of which corresponds to one of the transmission time slots and is configured to store at least one entry. The step further utilizes a linking of colliding transmission elements and movement of at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table. An illustrative technique is described in the specification, with reference to FIG. 7 of the drawings, at, for example, page 14, line 9 to page 16, line 12, wherein the traffic shaping requirement is a desired order of transmission.

Independent claim 22 is directed to an article of manufacture comprising a machine-readable storage medium for use in conjunction with a processor. The medium stores one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements, utilizing at least one time slot table comprising a plurality of locations, each of which corresponds to a transmission time slot and is configured to store at least one entry. The one or more programs when executed implement a step of establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements, and a step of scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more of the transmission time slots. The latter step makes use of a linking of colliding transmission elements and further involves moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table. In the illustrative embodiments described in the specification at, for example, page 5, lines 1-28, the article of manufacture comprising a machine-readable storage medium

may be, for example, internal memory 104 and/or external memory 106, as shown in FIGS. 1 and 2. This machine-readable storage medium contains one or more programs which, when executed on processor 102 as shown in FIGS. 1 and 2, implements the illustrative technique described in the specification, with reference to FIG. 7 of the drawings, at, for example, page 14, line 9 to page 16, line 12, wherein the traffic shaping requirement is a desired order of transmission.

The claimed invention provides a number of significant advantages over conventional arrangements. See the specification at, for example, page 3, lines 25-27 ("Advantageously, the techniques of the invention can accommodate multiple simultaneous collisions of transmission requests, and greatly facilitate the provision of QoS, CoS or other desired service levels for network connections.") and at page 4, lines 26-29 ("The present invention in an illustrative embodiment improves scheduling operations in a network processor or other processor through the use of a table-based scheduling technique which allows multiple transmission elements to be assigned to the same transmission time slot, while also maintaining a desired traffic shaping for the transmitted data blocks.")

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-15 and 18-20 stand rejected under 35 U.S.C. §103(a) over Patent No. 5,712,851 (hereinafter "Nguyen") in view of U.S. Patent No. 6,661,774 (hereinafter "Lauffenburger") and U.S. Patent No. 6,477,168 (hereinafter "Delp").

2. Claims 21 and 22 stand rejected under 35 U.S.C. §103(a) over Nguyen in view of Delp.

ARGUMENT

1. Claims 1-10 and 18-20

Appellants submit that the Nguyen, Lauffenburger and Delp references collectively fail to teach or suggest the limitations of independent claim 1. For example, the collective disclosure of Nguyen, Lauffenburger and Delp fails to teach or suggest "substantially maintain[ing] the traffic shaping requirement established by the traffic shaping circuitry in the presence of collisions

between requests from the transmission elements for each of one or more of the time slots . . . by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table," as recited in independent claim 1.

In formulating the rejection of claim 1, the Examiner acknowledges that neither Nguyen nor Lauffenburger disclose the above-quoted limitation, but argues that it is met by the teachings in Delp at column 6, lines 48-62. However, the limitation in question entails not merely moving at least one entry within a time slot table, but rather doing so in order to maintain a traffic shaping requirement in the presence of collisions between requests from transmission elements for each of one or more time slots.

Appellants respectfully submit that the relied-upon portion of Delp does not disclose moving an entry from one location of a time slot table to another in the presence of collisions between requests from the transmission elements and thus fails to teach or suggest the claim limitation. For example, Delp in conjunction with step 604 of FIG. 6 teaches to move a current time slot to a next time slot when no logical channel descriptor (LCD) is ready to be transmitted during the current time slot. Also, Delp in conjunction with step 606 of FIG. 6 teaches to reschedule an LCD responsive to a successful transmission. Neither of these operations involves moving an entry from one location of a time slot table to another in the presence of collisions between requests from the transmission elements, so as to substantially maintain a traffic shaping requirement, as recited in the independent claims of the present application.

With regard to the operation in step 604, Delp at column 6, lines 54-56 discloses "[w]hen an active bit ON for the current time is not identified, then a move to a next time slot is provided using one of multiple possible methods as indicated at a block 604" and at column 6, line 66 – column 7, line 4 discloses that, following a transmission, "when the next pointer is not active . . . a move to next time slot is performed at block 604." Thus, the "move to a next time slot" is performed only when an active bit is not set, indicating that no LCD is ready to be transmitted during that time slot and that the next time slot should be examined to see if any LCDs are ready to transmitted during that time. This corresponds with Delp, column 7, lines 6-32, which describes FIG. 7 as showing "exemplary steps for the move to the next time," which are performed only if the current time slot is empty.

With regard to the operation in step 606, Delp at column 6, lines 58-62 discloses that "when an active bit for the current time is identified, then the first LCD is prepared for transmission (TX), a next pointer from the LCD is saved and the LCD is rescheduled using one of multiple possible methods as indicated at a block 606." This rescheduling corresponds to the "comput[ing] the next time that this LCD has to be enqueued on the timing wheel" following "send[ing] out this cell or frame" as part of the "basic scheduling algorithm of cell/frame scheduler 102" discussed in Delp at column 6, lines 4-12. Appellants further submit that this corresponds to the "calculation of a new time stamp and a new time slot by the cell/frame scheduler 102" illustrated in FIG. 7A and discussed in column 7, lines 33-53 of Delp. As noted above, this move to another timeslot occurs only after a successful transmission and not in conjunction with collisions.

Accordingly, neither of the operations in steps 604 or 606 in Delp corresponds to the limitation of moving at least one entry in order to maintain a traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more time shots. The Nguyen and Lauffenburger references fail to supplement this fundamental deficiency of Delp. Accordingly, the limitation at issue is not taught or suggested by the proposed combination of references.

Appellants further submit that dependent claims 2-10 and 18-20 are allowable for at least the reasons identified above with regard to independent claim 1.

Claims 11-14

The additional limitation contained in dependent claim 11 regarding the use of a free pointer are neither taught nor suggested by the prior art cited by the Examiner. The Nguyen reference relied on by the Examiner in the rejection of claim 11 not only fails to disclose the use of a free pointer in the suggested manner, as conceded by the Examiner, but in fact actively teaches away from any use of a free pointer. See Nguyen at column 5, lines 22-29, which states as follows, with emphasis supplied: "[A] mechanism is introduced to 'look ahead' for empty cells. The look ahead mechanism requires that . . . the scheduler should . . . remember the first

non-empty slot." In other words, Nguyen suggests storing a pointer to the first non-empty cell rather than the first empty cell.

The Examiner relies on official notice without any evidentiary support for any use of a free pointer, much less the use of a free pointer in the manner claimed, as the primary grounds to reject claim 11. MPEP 2144.03 states that "It is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based." Appellants respectfully submit that the application of official notice to reject claims 11, in the absence of any evidentiary showing, fails to comply with this instruction.

Appellants further submit that, despite repeated requests to do so, Examiner has failed to provide either documentary evidence or an affidavit or declaration setting forth specific factual statements and explanation to support the invocation of official notice, as required by 37 C.F.R. §1.04(d)(2), in order for such a rejection to be maintained. Accordingly, Appellants submit that the rejection of claim 11 is improper and should be withdrawn.

Appellants further submit that claims 12-14 are allowable for at least the reasons identified above with regard to claim 11, from which they depend.

Claim 15

In addition to the argument above with regard to claim 15, from which it depends, the use of a free pointer claimed in dependent claim 15 is neither taught nor suggested by the prior art cited by the Examiner. The Nguyen reference relied on by the Examiner in the rejection of claim 15 not only fails to disclose the use of a free pointer in the suggested manner, as conceded by the Examiner, but in fact actively teaches away from any use of a free pointer. See Nguyen at column 5, lines 22-29, which states as follows, with emphasis supplied: "[A] mechanism is introduced to 'look ahead' for empty cells. The look ahead mechanism requires that . . . the scheduler should . . . remember the first non-empty slot." In other words, Nguyen suggests storing a pointer to the first non-empty cell rather than the first empty cell.

The Examiner relies on official notice without any evidentiary support for any use of a free pointer, much less the use of a free pointer in the manner claimed, as the primary grounds to

reject claim 15. MPEP 2144.03 states that "It is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based." Appellants respectfully submit that the application of official notice to reject claims 15, in the absence of any evidentiary showing, fails to comply with this instruction.

Appellants further submit that, despite repeated requests to do so, Examiner has failed to provide either documentary evidence or an affidavit or declaration setting forth specific factual statements and explanation to support the invocation of official notice, as required by 37 C.F.R. §1.04(d)(2), in order for such a rejection to be maintained. Accordingly, Appellants submit that the rejection of claim 15 is improper and should be withdrawn.

Appellants further submit that the limitation of claim 15 that states "wherein if the current pointer and the free pointer point to the same location in the time slot table and the actual pointer points to a different location in the time slot table, then the current pointer and the free pointer are both incremented to coincide with the actual pointer" is neither taught nor suggested by the combined references which fail to disclose any use of a free pointer at all. Moreover, Nguyen contains a further teaching away from the claim limitations. See Nguyen at column 5, lines 9-30, which states as follows, with emphasis supplied: "[W]hen the scheduler encounters an empty slot . . . . [and] the scheduler is backlogged, the scheduler should read the slots at the CCTP [current cell time pointer] and remember the first non-empty slot. When the current slot is serviced, the CSP [current slot pointer] of the scheduler should jump to this position." Accepting for the sake of argument Examiner's contention that the CCTP and CSP of Nguyen correspond to an actual pointer and current pointer, respectively (see the final Office Action at pages 6-7), Nguyen teaches that if the current pointer points to an empty slot (which would be the same as the free pointer if Nguyen implemented one) and the scheduler is backlogged (i.e., where the actual pointer points to different location in the time slot table than the current pointer, see Nguyen at column 4, lines 62-67), the actual pointer jumps to the position of the current pointer. This is diametrically opposed to the limitation of claim 15, wherein the current pointer and free pointer are both incremented to coincide with the actual pointer under similar circumstances.

Furthermore, with regard to motivation to modify Nguyen to meet the limitations of claim 15, the Examiner provides the following statement in the final Office Action at pages 7-8:

> It would have been obvious to one skilled in the art to increment a current pointer and free pointer to coincide with an actual pointer, if the current pointer and the free pointer point to the same location in the time slot table and the actual pointer points to a different location in the time slot table, since both the current and free pointer indicates the next slot to be transmitted and the actual pointer indicates the actual slot transmitting at that time. Thus, all pointers are pointing to a transmitting slot.

Appellants respectfully submit that the proffered statement fails to provide sufficient objective motivation for the combination. The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination "must be based on objective evidence of record" and that "this precedent has been reinforced in myriad decisions, and cannot be dispensed with." In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that "conclusory statements" by an Examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved "on subjective belief and unknown authority." Id. at 1343-1344. The statement listed above is believed to be a conclusory statement based on the type of "subjective belief and unknown authority" that the Federal Circuit has indicated provides insufficient support for an obviousness rejection.

2. Claims 21-22

Appellants submit that the Nguyen and Delp references collectively fail to teach or suggest the limitations of independent claim 21. For example, the collective disclosure of Nguyen and Delp fails to teach or suggest "substantially maintain[ing] the traffic shaping requirement established by the traffic shaping circuitry in the presence of collisions between requests from the transmission elements for each of one or more of the time slots . . . by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table," as recited in independent claim 21.

In formulating the rejection of claim 21, the Examiner acknowledges that Nguyen fails to disclose the above-quoted limitation, but argues that it is met by the teachings in Delp at column 6, lines 48-62. However, the limitation in question entails not merely moving at least one entry within a time slot table, but rather doing so in order to maintain a traffic shaping requirement in the presence of collisions between requests from transmission elements for each of one or more time slots.

Appellants respectfully submit that the relied-upon portion of Delp does not disclose moving an entry from one location of a time slot table to another in the presence of collisions between requests from the transmission elements and thus fails to teach or suggest the claim limitation. For example, Delp in conjunction with step 604 of FIG. 6 teaches to move a current time slot to a next time slot when no logical channel descriptor (LCD) is ready to be transmitted during the current time slot. Also, Delp in conjunction with step 606 of FIG. 6 teaches to reschedule an LCD responsive to a successful transmission. Neither of these operations involves moving an entry from one location of a time slot table to another in the presence of collisions between requests from the transmission elements, so as to substantially maintain a traffic shaping requirement, as recited in the independent claims of the present application.

With regard to the operation in step 604, Delp at column 6, lines 54-56 discloses "[w]hen an active bit ON for the current time is not identified, then a move to a next time slot is provided using one of multiple possible methods as indicated at a block 604" and at column 6, line 66 – column 7, line 4 discloses that, following a transmission, "when the next pointer is not active . . . a move to next time slot is performed at block 604." Thus, the "move to a next time slot" is performed only when an active bit is not set, indicating that no LCD is ready to be transmitted during that time slot and that the next time slot should be examined to see if any LCDs are ready to transmitted during that time. This corresponds with Delp, column 7, lines 6-32, which describes FIG. 7 as showing "exemplary steps for the move to the next time," which are performed only if the current time slot is empty.

With regard to the operation in step 606, Delp at column 6, lines 58-62 discloses that "when an active bit for the current time is identified, then the first LCD is prepared for transmission (TX), a next pointer from the LCD is saved and the LCD is rescheduled using one

of multiple possible methods as indicated at a block 606." This rescheduling corresponds to the "comput[ing] the next time that this LCD has to be enqueued on the timing wheel" following "send[ing] out this cell or frame" as part of the "basic scheduling algorithm of cell/frame scheduler 102" discussed in Delp at column 6, lines 4-12. Appellants further submit that this corresponds to the "calculation of a new time stamp and a new time slot by the cell/frame scheduler 102" illustrated in FIG. 7A and in discussed in column 7, lines 33-53 of Delp. As noted above, this move to another timeslot occurs only after a successful transmission and not in conjunction with collisions.

Accordingly, neither of the operations in steps 604 or 606 in Delp corresponds to the limitation of moving at least one entry in order to maintain a traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more time shots. The Nguyen reference fails to supplement this fundamental deficiency of Delp. Accordingly, the limitation at issue is not taught or suggested by the proposed combination of references.

Appellants further submit that independent claim 22 contains limitations similar to claim 21 and is thus allowable for at least the reasons identified above with regard to claim 21.

In view of the above, Appellants believe that claims 1-15 and 18-22 are in condition for allowance, and respectfully request the withdrawal of the §103(a) rejection.

Respectfully submitted,

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CLAIMS APPENDIX

1. A processor comprising:

scheduling circuitry for scheduling data blocks for transmission from a plurality of transmission elements; and

traffic shaping circuitry coupled to the scheduling circuitry and operative to establish a traffic shaping requirement for the transmission of the data blocks from the transmission elements;

wherein the scheduling circuitry is configured for utilization of at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to a transmission time slot and being configured to store at least one entry, the scheduling circuitry being operative in conjunction with the time slot table to schedule the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement established by the traffic shaping circuitry in the presence of collisions between requests from the transmission elements for each of one or more of the time slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

2. The processor of claim 1 wherein the time slot table is stored at least in part in an internal memory of the processor.

3. The processor of claim 1 wherein the time slot table is stored at least in part in an external memory coupled to the processor.

4. The processor of claim 1 wherein a given one of the locations in the time slot table stores an identifier of one of the transmission elements that has requested transmission of a block of data in the corresponding time slot.

5. The processor of claim 1 wherein one or more of the data blocks comprise data packets.

6. The processor of claim 1 wherein the established traffic shaping requirement is substantially maintained by linking together identifiers of transmission elements generating requests that collide for a given time slot, from a single entry in the corresponding table location, and then scheduling the requesting elements for transmission in the order in which they are linked.

7. The processor of claim 1 wherein the scheduling circuitry provides dynamic maintenance of the time slot table such that identifiers of requesting transmission elements are entered into the table locations on a demand basis.

8. The processor of claim 1 wherein identifiers of the transmission elements comprise a structure for allowing a given one of the transmission element identifiers to be linked to another of the transmission element identifiers.

9. The processor of claim 8 wherein in the event of a collision between multiple transmission elements requesting a given one of the time slots, an identifier of a first one of the requesting transmission elements is entered into the corresponding location in the time slot table, and that identifier is linked to an identifier of a second of the requesting transmission elements, with similar linking between the identifier of the second requesting transmission element and an identifier of any subsequent one of the requesting transmission elements, a linked list of the multiple requesting elements thereby being created for the corresponding location in the time slot table.

10. The processor of claim 9 wherein upon transmission of a data block from one of the requesting transmission elements in the linked list of elements, a determination is made as to whether there are any further elements linked to that element, and if there are any further elements, the identifier of the next such element is determined and that identifier is written into the corresponding location in the time slot table.

11. The processor of claim 1 wherein the scheduling circuitry maintains a set of pointers for the time slot table, the set of pointers comprising one or more of:

a current pointer pointing to the next location in the time slot table for which a data block will be transmitted;

an actual pointer pointing to the location in the time slot table corresponding to actual time; and

a free pointer pointing to the next location in the time slot table that is a free entry with no requesting transmission element assigned thereto.

12. The processor of claim 11 wherein in the event of a collision between multiple transmission elements requesting a given one of the time slots, a linked list of identifiers of the multiple requesting elements is created, and the current pointer continues to point to the corresponding location in the time slot table until each of the multiple requesting transmission elements has transmitted a data block.

13. The processor of claim 12 wherein the actual pointer advances by one table location for each of the data blocks transmitted.

14. The processor of claim 12 wherein the current pointer advances by one table location after each of the requesting transmission elements in the linked list associated with a given table location has transmitted a data block.

15. The processor of claim 12 wherein if the current pointer and the free pointer point to the same location in the time slot table and the actual pointer points to a different location in the

time slot table, then the current pointer and the free pointer are both incremented to coincide with the actual pointer.

18. The processor of claim 1 further comprising a transmit queue coupled to the scheduling circuitry and the traffic shaping circuitry, the transmit queue supplying time slot requests from transmission elements to the scheduling circuitry in accordance with the traffic shaping requirement established by the traffic shaping circuitry.

19. The processor of claim 1 wherein the processor comprises a network processor configured to provide an interface for data block transfer between a network and a switch fabric.

20. The processor of claim 1 wherein the processor is configured as an integrated circuit.

21. A method for use in a processor for scheduling data blocks for transmission from a plurality of transmission elements, the method comprising:

establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements; and

scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more transmission time slots, utilizing at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to one of the transmission time slots and being configured to store at least one

entry, and further utilizing a linking of colliding transmission elements and movement of at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

22. An article of manufacture comprising a machine-readable storage medium for use in conjunction with a processor, the medium storing one or more software programs for use in scheduling data blocks for transmission from a plurality of transmission elements, utilizing at least one time slot table, the time slot table comprising a plurality of locations, each of the locations corresponding to a transmission time slot and being configured to store at least one entry, wherein the one or more programs when executed implement the steps of:

establishing a traffic shaping requirement for the transmission of the data blocks from the transmission elements; and

scheduling the data blocks for transmission in a manner that substantially maintains the traffic shaping requirement in the presence of collisions between requests from the transmission elements for each of one or more of the transmission time slots, through the use of a linking of colliding transmission elements and by moving at least one entry from a first location within the at least one time slot table to a second location within the at least one time slot table.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None